AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): Fast Fourier Transforming apparatus for compensating an OFDM output bit signal, comprising:

an input buffer unit for storing and outputting a received OFDM bit signal;

a butterfly operation unit for performing a butterfly operation according to a radix algorithm at each stage;

a scale detection unit for calculating and outputting a scale factor which is a division factor used for controlling a bit value of a butterfly operated signal input from the butterfly operation unit to the input buffer unit at each stage within a predetermined bit limit of the received OFDM signal,

a scale count unit for cumulative counting a count coefficient corresponding to the scale factor input from the scale detection unit, and then outputting ~~the~~ a first result, and

a compensation unit for controlling the bit of a signal input from the butterfly operation unit according to values obtained from the scale detection and the scale count unit, and then outputting ~~the~~ a second result.

2. (currently amended): The Fast Fourier Transforming apparatus of claim 1, further comprising a first operation unit for dividing a bit value of a later input signal by the scale factor and outputting ~~the~~ a third result, thereby considering the scale factor from the scale detection unit when performing the butterfly operation.

3. (currently amended): The Fast Fourier Transforming apparatus of claim 1, further comprising an output buffer unit for storing a signal output from the butterfly operation unit at each of the stages and a control unit for controlling the signal stored in the output buffer unit to feed back to the input buffer unit until the butterfly operation is conducted as many times as the predetermined number of stages and outputting a butterfly operated signal at a final stage of the predetermined stages to the ~~bit-~~compensating unit.

4. (original) The Fast Fourier Transforming apparatus of claim 3, wherein a radix-2 algorithm is applied to the butterfly operation unit, the control unit controls the OFDM bit signal to be input to the input buffer unit by units of **8** bits and controls the predetermined bit limit of the scale detection unit to be set to **12** bits.

5. (original): The Fast Fourier Transforming apparatus of claim 4, wherein the scale factor is to be set to **4** if an absolute value of the butterfly operated bit signal is more than **1024**, to **2** if **512** and to **1** if **256** so that the butterfly operated bit value can be maintained at **8** bits.

6. (currently amended): The Fast Fourier Transforming apparatus of claim 5, wherein the scale count unit applies ~~4~~ **2** as the count figures if the scale factor from the scale detection unit is **4, 2**1 if **2** and ~~1~~**0** if ~~0~~**1** for cumulative counting the count figures corresponding to the scale factor.

7. (original): The Fast Fourier Transforming apparatus of claim 1, wherein the compensation unit compensates for the bit value of the input signal of the input buffer unit by the difference of the bit value of the predetermined number of stages and the input signal to the scale count unit.

8. (currently amended): The Fast Fourier Transforming apparatus of claim 7, wherein the compensation unit comprises,

a second operation unit for dividing the bit value of the butterfly operated output signal at the final stage of the predetermined stages by the scale factor calculated at the final stage,

a division and multiplication selection unit for calculating a difference value of the predetermined number of stages and an output value from the scale count unit, comparing the

predetermined number of stages with the output value from the scale count unit and outputting a selection data for division operation if the predetermined number of stages is greater or a selection signal for multiplication if the output value from the scale count unit is greater,

a ~~factor~~ coefficient calculation unit for calculating and outputting a quotient **Q** and a remainder **R** by dividing the difference value by **2**,

a division and multiplication calculation unit for dividing the value output from the second operation unit by 2^Q if the selection data is for the division operation while for multiplying the value output from the second operation unit by 2^Q if the selection data is for the multiplication operation,

a bit compensation unit for compensating the value output from the division and multiplication calculation unit according to the selection data from the division and multiplication selection unit and the remainder **R** from the coefficient calculation unit, and

an adder unit for adding the data input from the bit compensation unit and outputting the second result.

9. (original): The Fast Fourier Transforming apparatus of Claim 8, wherein the bit compensation unit outputs the data input from the division and multiplication calculation unit

intact if the remainder **R** is not **1**, where the remainder is calculated from the division of the difference value between the scale count value and the predetermined number of stages by **2**.

10. (original): The Fast Fourier Transforming apparatus of Claim 8, wherein the bit compensation unit multiplies the data input from the division and multiplication calculation unit by **1/2, 1/8, 1/16, 1/64,** respectively, if the remainder **R** is **1** and the selection data is for the division operation, thereby outputting each of the result value to the adder unit.

11. (original): The Fast Fourier Transforming apparatus of Claim 8, wherein the bit compensation unit multiplies the data input from the division and multiplication calculation unit by **1, 1/4, 1/8, 1/32**, respectively, if the remainder **R** is **1** and the selection data is for the multiplication operation, thereby outputting each of the result value to the adder unit.

12. (currently amended): The Fast Fourier Transforming apparatus of Claim 8, wherein the adder unit adds each of ~~the~~ 4 result values from the bit compensation unit to compensate for the bit of the input signal.

13. (currently amended): A Fast Fourier Transforming method for compensating an OFDM output bit signal, comprising:

a step of input buffering for storing and outputting a received OFDM bit signal,

a step of first operation for dividing the received signal by a scale factor and outputting ~~the~~ a first result,

a step of butterfly operation for butterfly operating on the first result at each of the stages according to a radix algorithm and outputting ~~the~~ a butterfly operated signal,

a step of scale detection for calculating the scale factor which is a division factor and is used for controlling the bit value of the butterfly operated signal to fall within the predetermined bit limit of the OFDM signal input at the step of the input buffering,

a step of scale counting for cumulatively counting a count figure corresponding to the scale factor of the input bit signal and outputting ~~the~~ a cumulative scale count value,

a step of feed back for repeating the step of input buffering through the step of scale count until a predetermined number of stages is reached, and

a step of compensation for controlling ~~the~~ a butterfly operated value, which is calculated at the final stage of a predetermined number of stages, according to the scale factor and the scale count value.

14. (original): The Fast Fourier Transforming method of Claim 13, further comprising a step of dividing a bit value of a later input signal by the scale factor and outputting

the divided result, thereby performing the butterfly operation in a manner of considering the scale factor.

15. (original): The Fast Fourier Transforming method of Claim 13, further comprising a step of output buffering for storing a signal resulting from the step of butterfly operation at each of the stages; and

a step of input/output control for controlling the signal stored at the step of output buffering to feed back to the step of input buffering until the butterfly operation is conducted as many times as the predetermined number of stages and passing the butterfly operated signal at the final stage of predetermined number of stages to the step of compensation.

16. (original): The Fast Fourier Transforming method of Claim 15, wherein, if a radix-2 algorithm is applied to the step of butterfly operation, the step of input/output control controls the OFDM bit signal to be passed to the step of input buffering by a unit of **8** bits and controls a predetermined bit limit to be set to **12** bits at the step of scale detection.

17. (original): The Fast Fourier Transforming method of Claim 16, wherein the scale factor is set to **4** if an absolute value of the butterfly operated bit signal is greater than **1024**, to **2** if **412** and to **1** if **256**, so that the butterfly operated bit value can be maintained at **8** bits.

18. (currently amended): The Fast Fourier Transforming method of claim 17, wherein at the step of scale counting, the number **4** is applied as the count factor if the scale factor is **4**, **2** if **2** and **1** if ~~0~~ 1 for cumulative counting the count figure corresponding to the scale factor.

19. (original): The Fast Fourier Transforming method of claim 13, wherein at the step of compensation, the bit value of the input signal of the step of input buffering is compensated by a difference of the bit value of the predetermined number of stages and the signal input from the step of scale count.

20. (currently amended): The Fast Fourier Transforming method of Claim 19, wherein the step of compensation comprises:

a step of a second operation for dividing the bit value of the butterfly operated output signal at the final stage of the predetermined number of stages by the scale factor calculated at the final stage;

a step of division and multiplication selection for calculating a difference value of the predetermined number of stages and the scale count value, comparing the predetermined number of stages with the scale count value and outputting a selection data for division operation if the predetermined number of stages is greater, while outputting a selection data for multiplication if the scale count value is greater;

a step of factor calculation for calculating and outputting a quotient **Q** and a remainder **R** by dividing the difference value by **2**;

a step of division and multiplication calculation for dividing the value resulting from the step of second operation by 2^Q if the selection data is for the division operation, while multiplying the value resulted from the step of second operation by 2^Q if the selection data is for the multiplication operation;

a step of bit compensation for compensating for the bit value resulting from the step of division and multiplication calculation according to the selection data and the remainder **R**; and

a step of adding for adding the bit data compensated at the step of bit compensation and outputting ~~the~~ a second result.

21. (original): The Fast Fourier Transforming method of Claim 20, wherein at the step of bit compensation, the data resulting from the step of division and multiplication calculation is output intact, if the remainder **R** is not **1**.

22. (original): The Fast Fourier Transforming method of Claim 20, wherein at the step of bit compensation, the data resulting from the step of division and multiplication calculation is multiplied by **1/2, 1/8, 1/16, 1/64**, respectively, if the remainder **R** is **1** and the

selection data is for the division operation, thereby passing each of the result values to the step of adding.

23. (original): Fast Fourier Transforming method of Claim 20, wherein at the step of bit compensation, the data resulting from the step of division and multiplication calculation is multiplied by **1/2, 1/4, 1/8, 1/32**, respectively, if the remainder **R** is **1** and the selection data is for the multiplication operation, thereby passing each of the result values to the step of adding.

24. (currently amended): The fast Fourier transforming method of Claim 20, wherein at the step of adding, each of ~~the~~ 4 result values from the step of bit compensation is added, thereby compensating for the bit of the input signal.